ICAR Laboratory Answers : HW Lab 1

Task 1

As script

Task 2

What logic state corresponds to the OPEN and CLOSED traps states?
OPEN = Logic '0'
CLOSED = Logic '1'

Task 3

What combination of switch positions will cause the Solenoid to be triggered?
Both switches need to be outputting a logic '1'

Task 4

What logic state causes the base LEDs to be illuminated?
LED on = Logic '1'
LED off = Logic '0'

What do the sensor output states ‘1’ and ‘0’ correspond to i.e. covered / uncovered?
Covered = Logic '1'
Uncovered = Logic '0'

Additional Task

the control logic's output signal (Enable) should be logically ANDed with the OSC signal. Then when the control logic enables the Solenoid this final AND gate's output will turn on / off as the OSC signal turns on / off i.e.

```
Solenoid = OSC AND Enable
```

Task 5

Which logic circuits implement a three input logical AND function? Which three input logical AND function has the shortest delay?

All are AND gates except circuit C.

The one with the shortest delay is dependent on the type of logic gates used. In general D should be fastest as it has the least gates, but does depend on how this gate is implemented.

Task 6

As script

Task 7

```
Solenoid = ((NOT LDR1 AND LDR2) OR (LDR1 AND NOT LDR2))
            OR
           (OSC AND  LDR1 AND LDR2)
```

Additional Task

```
A OR B = NOT ( (NOT A) AND (NOT B) )

A B  AORB  NOTA  NOTB  NOTA AND NOTB  NOT(NOTA AND NOTB)
0 0   0     1     1          1                  0
0 1   1     1     0          0                  1
1 0   1     0     1          0                  1
1 1   1     0     0          0                  1
```

Yes, it is possible, each OR gate is replaced with an AND gate and three NOT gates, as shown above, but its a lot more work :)

The back story, circuits and general bug related stuff refer to:

https://www-users.cs.york.ac.uk/~mjf/bug_trap/index.html