Systems and Devices 1 Lec 5c : The Computer

Before we get started ...

- We now have a "fully functioning" computer.
 - 12 instructions

Slide 2

- MOVE, LOAD, STORE
- ADD, SUB, ADDM, SUBM
- Bitwise-AND
- JUMP, JUMPZ, JUMPNZ
- 3 addressing modes, 2 data types
 - Immediate, Absolute, Direct.
 - Signed, Unsigned 8-bit data types.
- 256 x 16bit memory
 - 16-bit instructions, 8-bit variables
- What can we do with it? How can the computer interact with the real world?

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Slide 1

Instruction set

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		RTL	ENCODING ASSEMBLER
Move KK	:	ACC <- KK	0000 XXXX KKKKKKK MOVE 0x01
Add KK	:	ACC <- ACC + KK	0001 XXXX KKKKKKKK ADD 0x23
Sub KK	:	ACC <- ACC - KK	0010 XXXX KKKKKKKK SUB 0x45
And KK	:	ACC <- ACC & KK	0011 XXXX KKKKKKKK AND 0x67
Load AA	:	ACC <- M[AA]	0100 XXXX AAAAAAAA LOAD 0x89
Store AA	:	M[AA] <- ACC	0101 XXXX AAAAAAAA STORE 0x89
AddM AA	:	ACC <- ACC + M[AA]	0110 XXXX AAAAAAAA ADDM 0xAB
SubM AA	:	ACC <- ACC - M[AA]	0111 XXXX AAAAAAAA SUBM 0xAB
JumpU AA	:	PC <- AA	1000 XXXX AAAAAAAA JUMPU 0xCD
JumpZ AA	:	IF Z=1 PC <- AA	1001 XXXX AAAAAAAA JUMPZ 0xEF
		ELSE PC <- PC + 1	
JumpNZ AA	:	IF Z=0 PC <- AA	1010 XXXX AAAAAAAA JUMPNZ 0xF0
		ELSE PC <- PC + 1	

SimpleCPU machine-level instructions
 Everything has to be implement from these instructions

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Demo : System Test



1 # INSTR	IR15	IR14	IR13	IR12	IR11	IR10	IR09	IR08
2 # MOVE	0	θ	Θ	Θ	х	х	х	х
3 # ADD	0	θ	Θ	1	х	х	х	х
4 # SUB	0	0	1	0	х	x	х	х
5 # AND	0	θ	1	1	х	х	х	х
6 # LOAD	0	1	Θ	0	х	х	х	х
7 # STORE	0	1	Θ	1	х	х	х	х
8 # JUMPU	1	0	Θ	0	х	х	х	х
9 # JUMPZ	1	θ	Θ	1	х	х	х	х
10 # JUMPNZ	1	θ	1	Θ	х	х	х	х
11								
12 # ACC BIT	TEST							
13 #								
14								
15 00 move	0x00							
16 01 move	0x01							
17 02 move	0x02							
18 03 move	0x04							
19 04 move	0x08							
20 05 move	0x10							
21 06 move	0x20							
22 07 move	0x40							
23 08 move	0x80							
24 09 move	0x40							
25 10 move	0x20							
26 11 move	0x10							
27 12 move	0x08							
28 13 move	0x04							
29 14 move	0x02							
30 15 move	0x01							
21	_						_	

- Before we can write our "first" program we need to test if the hardware is working correctly e.g. are there any damaged ICs or missing wires, ...
- Therefore, our first program is a test program: test.asm
 - Lets go through the code ...

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Demo : Hello World

- Traditionally the first program you write on any new machine is one that prints "Hello World".
 - The FPGA board used to implement SimpleCPU does not have a display

Serial terminal

Two choices:

I CD



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GPIO

- To interface the processor to the outside world we commonly use General Purpose Input Output pins.
 - Programmer controlled digital interface devices that can read inputs and control outputs in the real world.
 - Software controlled IO, no hardware support.
- Alternatively, application specific peripheral devices:
 - Parallel Port : data transferred using multiple wires e.g. comparable to a bus inside the processor, additional hardware support to synchronise data transfers, buffer data.
 - Serial Port : data transferred using a single wire i.e. one bit at a time, additional hardware support to convert parallel data to serial and vice versa, hardwired control logic, data buffers etc.
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- Memory mapped (address 0xFF) output port
 8 bit register, Q outputs drive external signals connected
 - to LCD display





 Address decoding logic only enables output register when the processor writes to address 0xFF.

Q outputs updated with value on DATA_OUT bus (bits 7:0) University of York : M Freeman 2021

Parallel Port



Memory Map									
0xFF	GPO								
0xFE									
	RAM								
0x00									

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- Quick Quizz (be careful trick question)
 - Can the processor read the output of the parallel port?
 - What happens when the CPU writes to ADDR 0xFF?
 - What happens when the CPU reads from ADDR 0xFF? University of York : M Freeman 2021

Text characters

	Decimal	Hex	Char	Decimal	Hex	Char	Decimal	Hex	Char	Decimal	Hex	Char
	0	0	[NULL]	32	20	[SPACE]	64	40	0	96	60	× .
	1	1	[START OF HEADING]	33	21	1	65	41	Α	97	61	а
	2	2	[START OF TEXT]	34	22		66	42	в	98	62	b
	3	3	[END OF TEXT]	35	23	#	67	43	с	99	63	с
	4	4	[END OF TRANSMISSION]	36	24	\$	68	44	D	100	64	d
	5	5	[ENQUIRY]	37	25	%	69	45	E	101	65	е
	6	6	[ACKNOWLEDGE]	38	26	&	70	46	F	102	66	f
	7	7	[BELL]	39	27	1.1	71	47	G	103	67	q
	8	8	[BACKSPACE]	40	28	(72	48	н	104	68	ĥ
	9	9	[HORIZONTAL TAB]	41	29)	73	49	1	105	69	1
	10	Α	[LINE FEED]	42	2A	*	74	4A	J	106	6A	i
	11	В	[VERTICAL TAB]	43	2B	+	75	4B	ĸ	107	6B	k
	12	С	[FORM FEED]	44	2C	,	76	4C	L	108	6C	1
	13	D	[CARRIAGE RETURN]	45	2D	-	77	4D	M	109	6D	m
	14	E	[SHIFT OUT]	46	2E		78	4E	N	110	6E	n
	15	F	[SHIFT IN]	47	2F	1	79	4F	0	111	6F	0
	16	10	[DATA LINK ESCAPE]	48	30	0	80	50	P	112	70	D
	17	11	[DEVICE CONTROL 1]	49	31	1	81	51	Q	113	71	q
	18	12	[DEVICE CONTROL 2]	50	32	2	82	52	R	114	72	r i i i i i i i i i i i i i i i i i i i
	19	13	[DEVICE CONTROL 3]	51	33	3	83	53	S	115	73	S
	20	14	[DEVICE CONTROL 4]	52	34	4	84	54	т	116	74	t
	21	15	[NEGATIVE ACKNOWLEDGE]	53	35	5	85	55	U	117	75	u
	22	16	[SYNCHRONOUS IDLE]	54	36	6	86	56	v	118	76	v
100	23	17	[ENG OF TRANS. BLOCK]	55	37	7	87	57	w	119	77	w
	24	18	[CANCEL]	56	38	8	88	58	х	120	78	x
	25	19	[END OF MEDIUM]	57	39	9	89	59	Y	121	79	v
	26	1A	[SUBSTITUTE]	58	ЗA	1.0	90	5A	z	122	7A	z
	27	1B	[ESCAPE]	59	3B	;	91	5B	E I	123	7B	{
	28	1C	[FILE SEPARATOR]	60	3C	<	92	5C	Λ	124	7C	- É
	29	1D	[GROUP SEPARATOR]	61	3D	=	93	5D	1	125	7D	}
	30	1E	[RECORD SEPARATOR]	62	3E	>	94	5E	^	126	7E	~
	31	1F	[UNIT SEPARATOR]	63	3F	?	95	5F	-	127	7F	[DEL]
പ		0	E alaba a		0 10	- 2	2		tral	aha		otor
5		9	n-Isnolis c		er	C. 3	5 C(וחנ	ποι	cna	ra I	ciers
		1.1.										

Used in a later lab.

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110 us 120 us 130 us lla cik r 駴 dout[7:0 6] U. [5] 6 [4] կել [1] 17. [O] Ug e Ug rs DAT O BLANK W F 0 R

LCD module is controlled using a 6 bit bus

- E (7) : enable, active high, indicates that RS and DATA lines are valid and can be read.
- ▶ RS (6) : register select, 0 = command, 1 = character data
- Data (5:2) : 4 bit data bus, chars transferred as two nibbles.

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Demo : Hello World

1	#												
2	#	INTERF/	ACE										
3	#												
4													
5	#	07.	11	F	*	/							
6	#	06.	1,	+ RS	*	1							
7	#	05.	1,	+ D7	*	1							
8	#	04.	1,	* D6	*	1							
9	#	03.	1,	+ D5	*	1							
10	#	02.	1,	+ D4	*	1							
11	#	01.	1,	+ N∐	*	1							
12	#	00.	1,	+ NU	*	1							
13		ų.,	'										
14	#	Initia	li¢	e d	isi	n la	,						
15	#												
16													
17	st	art:											
18	3	move		0×0	A	#	10:	ь	AC	<u>،</u>	i t	he	
19		store		0x6	F	#	wri	1	- t		int.		, port
20		31011	-	0.01		"					uc	put	. por c
21	#	0011 00	a 11		i + i	ali	60						
22	#												
23	"												
24	#		F	RS	דס	D6	L r	15	D4	x	x		
25	#	0011 -	ē	0	6	6	11	í	1	A	6	-	0,000
26	#	0011 -	õ	0	Ā	Ä	14	ì	1	A	0	-	0x0C
27	"	0011	0	0	•	•			-	0	0	-	UNUC
28		move		0×0	c	#	tra		fe	r A	01	1	
29		store		AVE	Ē	#	wri	+	5 t		int.	t	nort
30		add	~	0x8	Θ	#	set	- 1	= h	inh		200	
31		stor		AYE	Ē	#	wri	+			+	nut	nort
32		sub	-	018	A	#	set	- 1	÷ 1.	0.0	υĽ	PUL	
22		300		200	ž		301	. '					



 Software defined parallel port
 Bit flipping of control lines, bitwise operations etc. University of York : M Freeman 2021

Parallel Port

Worked Example : SimpleCPU_PIO



Parallel IO (PIO)

Run-time : approximately 700 us at 10MHz University of York : M Freeman 2021

Worked Example : SimpleCPU_PIO

13	
14	# Initialise display
15	#
16	
17	start:
18	move 0x00 # load ACC with 0
19	store 0xFF # write to output port
20	
21	# 0011 0011 Initialise
22	#
23	
24	# E RS D7 D6 D5 D4 X X
25	# 0011 - 0 0 0 0 0 1 1 0 0 = 0x0C
26	$# 0011 - 0 0 0 0 1 1 0 0 = 0 \times 0 C$
27	_
28	move 0x0C # transfer 0011
29	store 0xFF # write to output port
30	add 0x80 # set E high
31	store 0xFF # write to output port
32	sub 0x80 # set E low
33	store 0xFF # write to output port
34	
35	move 0x0C # transfer 0011
36	store 0xFF # write to output port
37	add 0x80 # set E high
38	store WXFF # write to output port
39	SUD UX80 # Set E LOW
40	store WXFF # write to output port

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185	#	0100 1	000 Pr	rint	'H'				
186	#								
187									
188	#		E RS	D7 [06 D	5 D4	1 X	Х	
189	#	0100 -	0 1	0 1	ιjο	Θ	0	0 =	= 0×50
190	#	1000 -	01	1 6	e je	Θ	0	0 =	= 0x60
191									
192		move	0x50	#	trans	fer	010	0	
193		store	0xFF	#	write	to	out	put	port
194		add	0x80	#	set E	hig	jh		
195		store	0xFF	#	write	to	out	put	port
196		sub	0x80	#	set E	lov	1		
197		store	0xFF	#	write	to	out	put	port
198								-	
199		move	0x60	#	trans	fer	100	0	
200		store	0xFF	#	write	to	out	put	port
201		add	0x80	#	set E	hig	jh		
202		store	0xFF	#	write	to	out	put	port
203		sub	0x80	#	set E	lov	1		
204		store	0xFF	#	write	to	out	put	port
205								-	

.data 0 Other:

.data 0

• Lets go through the code

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Worked Example : SimpleCPU_PIO



Alternative implementation using MACROs

We will look at the M4 pre-processor in a later Lecture/Lab University of York : M Freeman 2021

Programming structures



of code, missing: selection and iteration (lab6).
 Identify character, 0=False, 1=True.
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Serial data link, two wire interface: RxD, TxD + GND

- ASCII data converted into a serial data packet e.g. letter "H"
 - Packet divided into equal time slices, each bit allocated one slice.
 - Communications speed, bits per second (bps) e.g. 300bps = 3.3ms
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Worked Example : SimpleCPU_SIO



- Serial IO (SIO)
 - Run-time : approximately 300ms at 10MHz University of York : M Freeman 2021

Hello World



Serial Port

• Pseudo code

and flowchart

each BIT

each CHAR

Need to:

Select

Select

data = message[i]
while data != NULL:
 set serialLine low
 wait 3.3ms

for j in range 0 to 7:
 set serialLine data[j]
 wait 3.3ms
set serialLine high
wait 3.3ms

i = i + 1 data = message[i]

i: .data 0

j: .data 0

data: .data 0

message:

.data `H','E','L','L','O',' ` .data `W','O','R','L','D','\O`



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	0100 100	0	=	0x48	= 'H	['
				TX ST	ART	
	0100 100) ()	=	TX 0	=	0x48
shift right	0010 010	0	=	ТХ О	=	0x24
shift right	0001 001	. 0	=	TX 0	=	0x12
shift right	0000 100) 1	=	TX 1	=	0x09
shift right	0000 010) ()	=	ТΧ Ο	=	0x04
shift right	0000 001	. 0	=	TX 0	=	0x02
shift right	0000 000) 1	=	TX 1	=	0x01
shift right	0000 000	0	=	ТΧ Ο	=	0x00
-				TX ST	OP	

Select BIT

• Q: how can we shift ASCII data in the ACC right?

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Serial Port

- A : write a program to divide the character data by 2 e.g. simple repeated subtraction.
 - Count how many times 2 can be subtracted without generating a carry.
- Q : how can we read character data from memory i.e. implement data = message[i]
- A : we can not i.e. at the moment we only have an absolute addressing mode LOAD instruction.
 - Read address can not be changed at runtime e.g. LOAD 55, we can not use a variable to address memory i.e. M[i].
 - However, we can bodge this by using self modifying code :)

Memory : Load / Store



For the simpleCPU_v1a we take the simple solution

Only read and write to lower 8-bits of a memory locations, downside wastes memory i.e. each time you declare a variable we will waste 8-bits.

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SimpleCPU_v1a



• Set the high byte of data_out = 0x00 University of York : M Freeman 2021

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SimpleCPU_v1a



• Set the high byte of data_out = 0x00 University of York : M Freeman 2021

SimpleCPU_v1a



• Set the high byte of data_out = 0x40 University of York : M Freeman 2021

Quick Quizzz

start: load message store char load start add 1 store start jump start	# # # # # #	ADDRESS 0 1 2 3 4 5	DATA 0x4007 0x5006 0x4000 0x1001 0x5000 0x8000
char:		<i>.</i>	
.data 0	#	6	0x0000
message:			
.data `H'	#	7	0x0048
.data `E'	#	8	0x0045
.data `L'	#	9	0x004C
.data `L'	#	10	0x004C
.data 'O'	#	11	0x004F

If we did hardwire the data_out bus to 0x40 || ACC, what does the above code do?

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SimpleCPU_v1a

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Set the high byte of data_out = IR[11:8] || 0000

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SimpleCPU_v1a

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SimpleCPU v1a



 Self-modifying code, what can go wrong :)
 "New" 2-operand STORE instruction University of York : M Freeman 2021

A Wheeler JUMP

DATA = 22 X = FUNC(DATA) FUNC: RETURN DATA×2	CODE: MOVE CODE JUMP FUNC 	10 MOVE 10 11 JUMP 50 12
	FUNC: ADD 2 STORE 8 EXIT LOAD DATA ADDM DATA EXIT: JUMP EXIT DATA: 22	50 ADD 2 51 STORE 8 54 52 LOAD 55 53 ADDM 55 54 JUMP 54 55 22

The first implementation of a function call.
 Quick Quizz : how does this code work?

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Worked Example : SimpleCPU_SIO

simpleCPUv1a.m4 (~/Documents/SYS1_2021/5	ides/LEC_05/ODP/Code) - + ×	514 C.4	*hello_wo	orld_seria	l.asm (~/Do	cumen	ts/SYS	51_2021/Slides/LEC	_05/ODP/Code) -	- + >
		File Edi	view Sea	arcn 100	is Documer	nts Hel	p			
		р (с		~ 5	% D	0	Q C	2		
4 define(delay, 5 move \$1 6 store \$2 7 8 delayLoop\$3: 9 move 0 11 minerLoop\$3 12 jump2 outerLoop\$3 13 jump innerLoop\$3 14 15 outerLoop\$3: 16 load \$2 17 sub 1 1 store \$2 10 jumpnz delayLoop\$3' 21 22 define(shiftRight, '23 23 move 0 24 store \$1 25 divloop\$2 26 jumon div exit 27 move 0 28 store \$2 29 and 0x80 30 jumpnz div exit 31 store \$2 26 load \$1 33 store \$1 34 jum div_exit 35 load \$1 36 jump. div_exit 31 store \$2 36 jump. div_exit 37 store \$2' 38 jum div_exit 36 jump. div_exit 37 store \$2' 38 jum		63 # \ 64 65 chi 66 67 txt 68 67 txt 68 67 txt 68 70 d 71 dei 72 73 tm 74 73 tm 74 73 tm 74 76 # [77 m] 78 mes 79 80 81 82 83 84 85 87 89 90 91 92 93 93	ARIABLU i.data Juff: 	ES 0 0 0 0 0 0 0 0 0 0 0 0 0	RS TO D	ISPLA # H # L # L # U # W # W # W # W # W # C R # NUL Plain	IY 	01001000 01000101 0100100 0100100 010010	105 61	
m4 ▼ Tab	Vidth: 4 👻 Ln 23, Col 9 INS		_	_	_	Halli	Text •	100 Wilder. 4 •	Li 90, COTT	114

• Lets go through the code ... University of York : M Freeman 2021

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Worked Example : UART



Universal Asynchronous Receiver Transmitter unit
 A hardware implemented serial port

University of York : M Freeman 2021

Worked Example : UART



- Three memory mapped registers
 - TX data : write only, triggers automatic TX of value
 - RX data : read only, return received 8bit value (ASCII char)
 - Status : read only, return status of RX, TX and Buffer.

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Worked Example : UART

4 4			26 start:
1 #	F MEMORY MAP		
2 #	# 0xFF - WR - UART tx		
3 #	≠ 0xFF - RD - UART Γx		28 STORE WXFF
4 #	≠ 0xFE - WR - UART tx	4	29
5 #	AXEE - RD - MART status		30 wait1:
6	ONTE NO ONNI Status	3	31 load 0xFE # wait for TX
7 +	AVED UP CDTO autout		32 and 0x04
1 #	F OXFD - WR - GPIO OULDUL		33 jumpz wait1
8#	F 0XFD - RD - GPIO input	Sector 2	
9 #	# 0xFC - WR - GPIO output		
10 #	# 0xFC - RD - GPIO input		ss toop:
11		-	36 load 0xFE # wait for RX
12 #	# UART REGISTERS	1	37 and 0x01
13 #	t TX : B7 - B0 data	3	38 jumpz loop
14 ±	t RX · B7 - B0 data	3	39
15		4	40 load 0xFF # read RX
16 4		4	41 store 0xFF # wait RX to TX
10 #	F STATUS REGISTER		12 store AvED
1/ #	F B7 : NU		
18 #	‡ B6 : NU	í í	+3 44
19 #	# B5 : NU	é de la companya de	44 waitz:
20 #	‡ B4 : NU	4	45 load 0xFE # wait for IX
21 #	# B3 : NU	4	46 and 0x04
22 ±	B2 : TX Tdle	4	47 jumpz wait2
23 #	t B1 · BX Idle	4	48
24 +		4	49 jump start
24 #	P DU ; KA Vallu		50
25			

• Lets go through the code ... A lot simpler when its all done in hardware :) University of York : M Freeman 2021

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10 #

16 # 17 # 18 #

19 # 20 # 21 #

22 # 23 #

24 #

11 12 # 13 #

Summary

Key concepts

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- Control logic
 - Representing processor state
 - Generating control signals
- Character (text) data types : ASCII
- Parallel and Serial ports (IO)
 - Memory maps and memory mapped devices
- Assembly language programming
 - Three case studies:
 - Easy : multiply 10 by 3
 - Medium : Hello World LCD
 - Hard : Hello World Serial (covered again in lab)

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