8. Cyclone II Memory Blocks

CII51008-2.4

Introduction

Cyclone® II devices feature embedded memory structures to address the on-chip memory needs of FPGA designs. The embedded memory structure consists of columns of M4K memory blocks that can be configured to provide various memory functions such as RAM, first-in first-out (FIFO) buffers, and ROM. M4K memory blocks provide over 1 Mbit of RAM at up to 250-MHz operation (see Table 8–2 on page 8–2 for total RAM bits per density).

Overview

The M4K blocks support the following features:

- Over 1 Mbit of RAM available without reducing available logic
- 4,096 memory bits per block (4,608 bits per block including parity)
- Variable port configurations
- True dual-port (one read and one write, two reads, or two writes) operation
- Byte enables for data input masking during writes
- Initialization file to pre-load content of memory in RAM and ROM modes
- Up to 250-MHz operation

Table 8–1 summarizes the features supported by the M4K memory.

Table 8–1. Summary of M4K Memory Features (Part 1 of 2)

Feature	M4K Blocks
Maximum performance *(1)*	250 MHz
Total RAM bits (including parity bits)	4,608
Configurations	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36
Parity bits	✓
Byte enable	✓

Table 8–1. Summary of M4K Memory Features (Part 2 of 2)	
Feature	**M4K Blocks**
Packed mode	✓
Address clock enable	✓
Single-port mode	✓
Simple dual-port mode	✓
True dual-port mode	✓
Embedded shift register mode *(2)*	✓
ROM mode	✓
FIFO buffer *(2)*	✓
Simple dual-port mixed width support	✓
True dual-port mixed width support	✓
Memory Initialization File (**.mif**)	✓
Mixed-clock mode	✓
Power-up condition	Outputs cleared
Register clears	Output registers only
Same-port read-during-write	New data available at positive clock edge
Mixed-port read-during-write	Old data available at positive clock edge

Notes to Table 8–1:
(1) Maximum performance information is preliminary until device characterization.
(2) FIFO buffers and embedded shift registers require external logic elements (LEs) for implementing control logic.

Table 8–2 shows the capacity and distribution of the M4K memory blocks in each Cyclone II device family member.

Table 8–2. Number of M4K Blocks in Cyclone II Devices (Part 1 of 2)		
Device	**M4K Blocks**	**Total RAM Bits**
EP2C5	26	119,808
EP2C8	36	165,888
EP2C15	52	239,616
EP2C20	52	239,616
EP2C35	105	483,840

Table 8–2. Number of M4K Blocks in Cyclone II Devices (Part 2 of 2)		
Device	**M4K Blocks**	**Total RAM Bits**
EP2C50	129	594,432
EP2C70	250	1,152,000

Control Signals

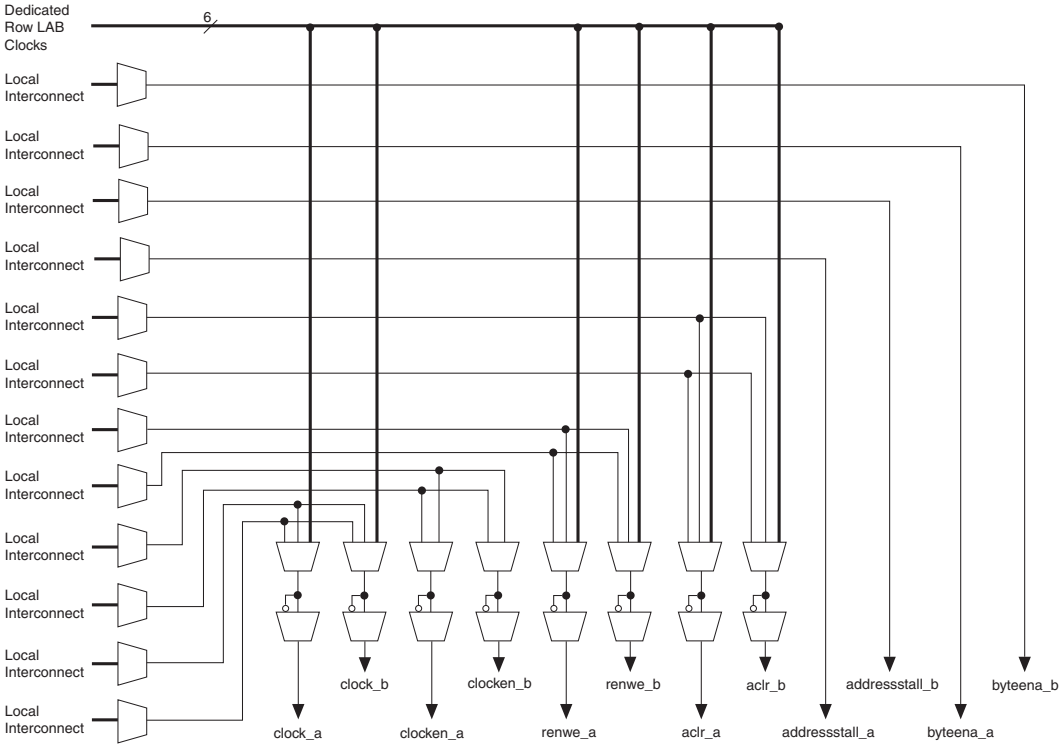
Figure 8–1 shows how the register clocks, clears, and control signals are implemented in the Cyclone II memory block.

The clock enable control signal controls the clock entering the entire memory block, not just the input and output registers. The signal disables the clock so that the memory block does not see any clock edges and will not perform any operations.

Cyclone II devices do not support asynchronous clear signals to input registers. Only output registers support asynchronous clears. There are three ways to reset the registers in the M4K blocks: power up the device, use the `aclr` signal for output register only, or assert the device-wide reset signal using the `DEV_CLRn` option.

When applied to output registers, the asynchronous clear signal clears the output registers and the effects are seen immediately.

Figure 8–1. M4K Control Signal Selection



Parity Bit Support

Error detection using parity check is possible using the parity bit, with additional logic implemented in LEs to ensure data integrity. Parity-size data words can also be used for other purposes such as storing user-specified control bits.

Refer to the *Using Parity to Detect Errors White Paper* for more information.

Byte Enable Support

All M4K memory blocks support byte enables that mask the input data so that only specific bytes of data are written. The unwritten bytes retain the previous written value. The write enable (`wren`) signals, along with the byte enable (`byteena`) signals, control the RAM block's write operations. The default value for the byte enable signals is high (enabled), in which

case writing is controlled only by the write enable signals. There is no clear port to the byte enable registers. M4K blocks support byte enables when the write port has a data width of 1, 2, 4, 8, 9, 16, 18, 32, or 36 bits. When using data widths of 1, 2, 4, 8, and 9 bits, the byte enable behaves as a redundant write enable because the data width is less than or equal to a single byte. Table 8–3 summarizes the byte selection.

Table 8–3. Byte Enable for Cyclone II M4K Blocks *Note (1)*

byteena[3..0]	Affected Bytes								
	datain ×1	datain ×2	datain ×4	datain ×8	datain ×9	datain ×16	datain ×18	datain ×32	datain ×36
[0] = 1	[0]	[1..0]	[3..0]	[7..0]	[8..0]	[7..0]	[8..0]	[7..0]	[8..0]
[1] = 1	-	-	-	-	-	[15..8]	[17..9]	[15..8]	[17..9]
[2] = 1	-	-	-	-	-	-	-	[23..16]	[26..18]
[3] = 1	-	-	-	-	-	-	-	[31..24]	[35..27]

Note to Table 8–3:
(1) Any combination of byte enables is possible.

Table 8–4 shows the byte enable port control for true dual-port mode.

Table 8–4. Byte Enable Port Control for True Dual-Port Mode

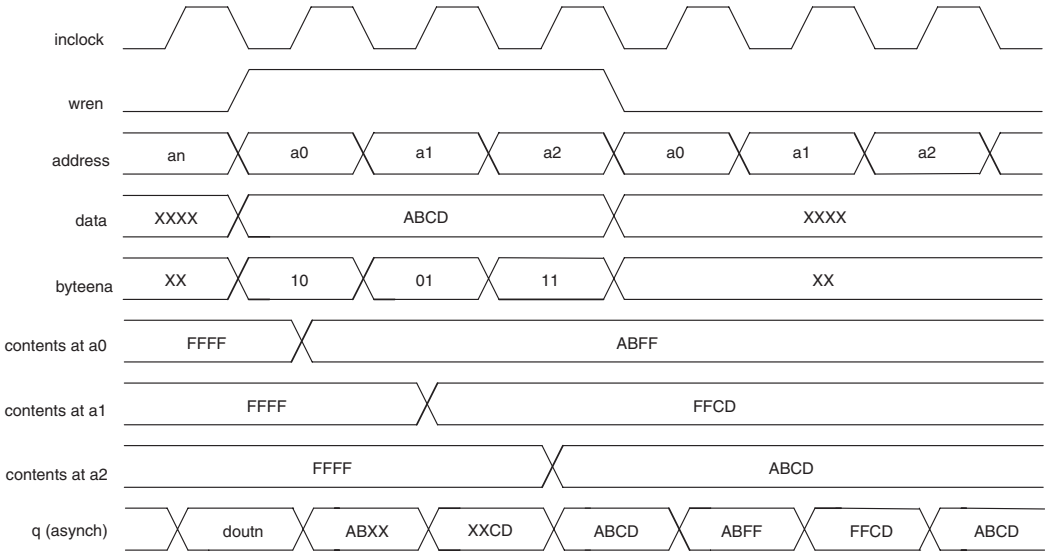
byteena [3:0]	Affected Port
[1:0]	Port A *(1)*
[3:2]	Port B *(1)*

Note to Table 8–4:
(1) For any data width up to ×18 for each port.

Figure 8–2 shows how the `wren` and `byteena` signals control the operations of the RAM.

When a byte enable bit is de-asserted during a write cycle, the corresponding data byte output appears as a "don't care" or unknown value. When a byte enable bit is asserted during a write cycle, the corresponding data byte output is the newly written data.

Figure 8–2. Cyclone II Byte Enable Functional Waveform



Packed Mode Support

Cyclone II M4K memory blocks support packed mode. You can implement two single-port memory blocks in a single block under the following conditions:

- Each of the two independent block sizes is less than or equal to half of the M4K block size. The maximum data width for each independent block is 18 bits wide.
- Each of the single-port memory blocks is configured in single-clock mode.

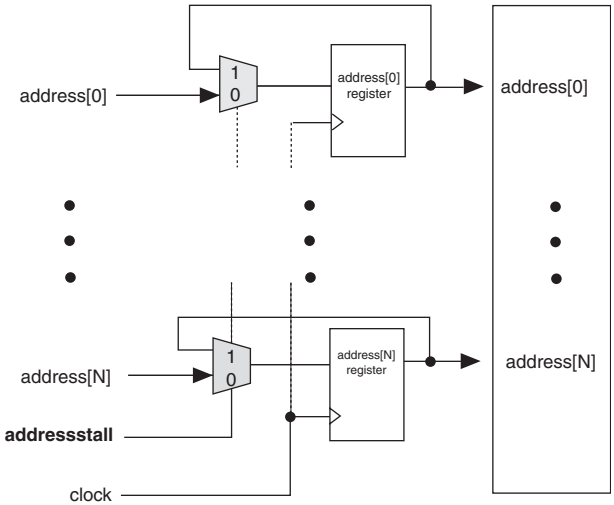
See "Single-Port Mode" on page 8–9 and "Single-Clock Mode" on page 8–24 for more information.

Address Clock Enable

Cyclone II M4K memory blocks support address clock enables, which holds the previous address value until needed. When the memory blocks are configured in dual-port mode, each port has its own independent address clock enable.

Figure 8–3 shows an address clock enable block diagram. The address register output is fed back to its input via a multiplexer. The multiplexer output is selected by the address clock enable (`addressstall`) signal. Address latching is enabled when the `addressstall` signal goes high (active high). The output of the address register is then continuously fed into the input of the register until the `addressstall` signal goes low.

Figure 8–3. Cyclone II Address Clock Enable Block Diagram



The address clock enable is typically used for cache memory applications to improve efficiency during a cache-miss. The default value for the address clock enable signals is low (disabled). Figures 8–4 and 8–5 show the address clock enable waveforms during the read and write cycles, respectively.

Figure 8–4. Cyclone II Address Clock Enable During Read Cycle Waveform

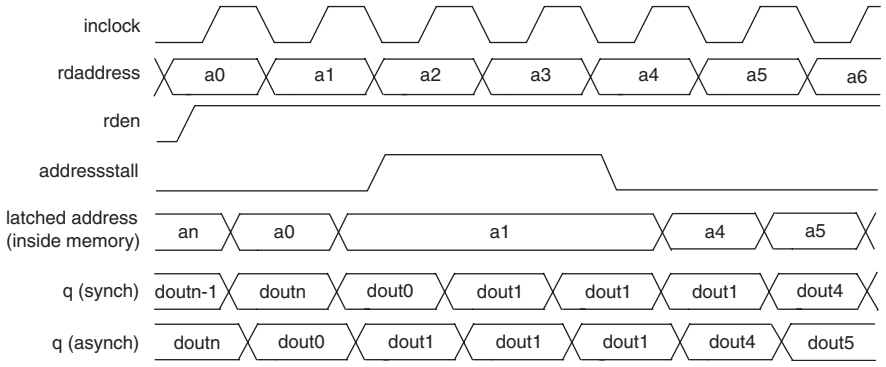
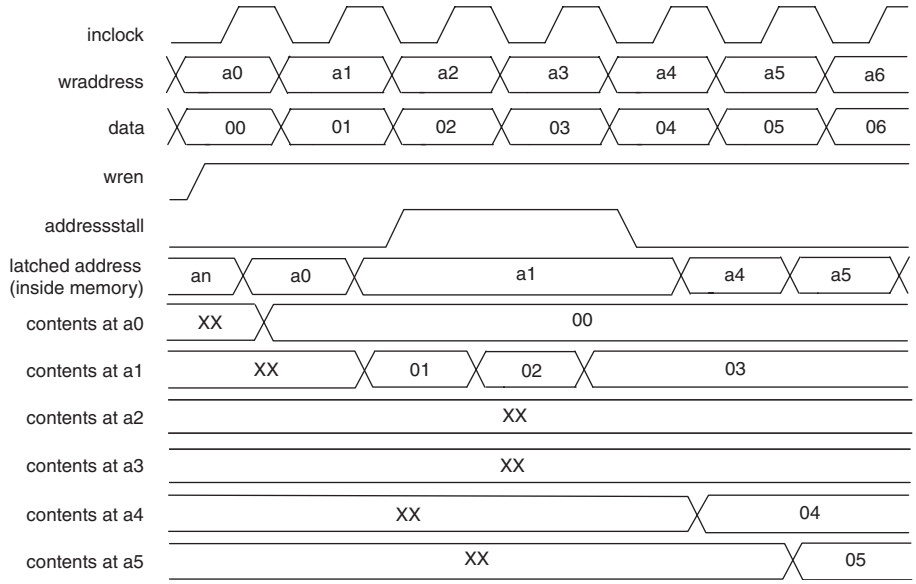


Figure 8–5. Cyclone II Address Clock Enable During Write Cycle Waveform



Memory Modes

Cyclone II M4K memory blocks include input registers that synchronize writes and output registers to pipeline data, thereby improving system performance. All M4K memory blocks are fully synchronous, meaning that you must send all inputs through a register, but you can either send outputs through a register (pipelined) or bypass the register (flow-through).

M4K memory blocks do not support asynchronous memory (unregistered inputs).

The M4K memory blocks support the following modes:

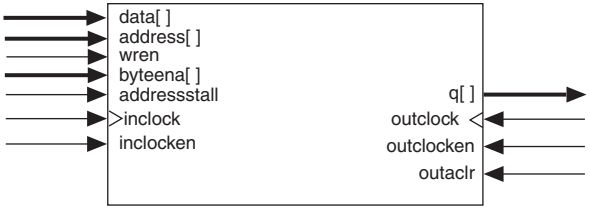
- Single-port
- Simple dual-port
- True dual-port (bidirectional dual-port)
- Shift register
- ROM
- FIFO buffers

Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

Single-Port Mode

Single-port mode supports non-simultaneous read and write operations. Figure 8–6 shows the single-port memory configuration for Cyclone II memory blocks.

Figure 8–6. Single-Port Mode *Note (1)*



Note to Figure 8–6:
(1) Two single-port memory blocks can be implemented in a single M4K block in packed mode.

In single-port mode, the outputs are in read-during-write mode, which means that during the write operation, data written to the RAM flows through to the RAM outputs. When the output registers are bypassed, the new data is available on the rising edge of the same clock cycle on which it was written.

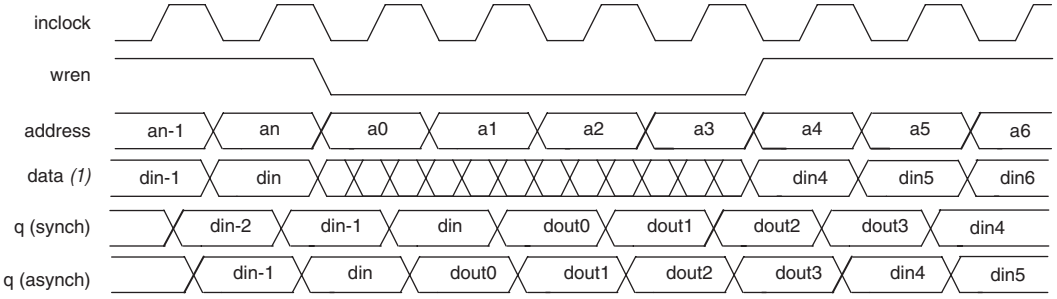
See "Read-During- Write Operation at the Same Address" on page 8–28 for more information about read-during-write mode.

The port width configurations for M4K blocks in single-port mode are as follows:

- 4K × 1
- 2K × 2
- 1K × 4
- 512 × 8
- 512 × 9
- 256 × 16
- 256 × 18
- 128 × 32
- 128 × 36

Figure 8–7 shows timing waveforms for read and write operations in single-port mode.

Figure 8–7. Cyclone II Single-Port Timing Waveforms

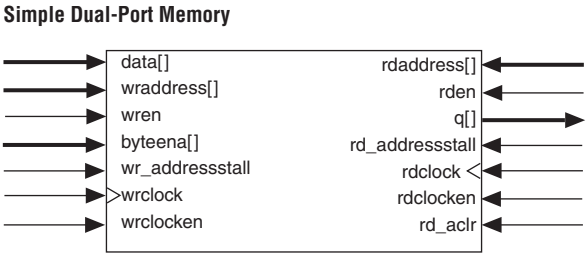


Note to Figure 8–7:
(1) The crosses in the `data` waveform during read mean "don't care."

Simple Dual-Port Mode

Simple dual-port mode supports simultaneous read and write operation. Figure 8–8 shows the simple dual-port memory configuration.

Figure 8–8. Cyclone II Simple Dual-Port Mode *Note (1)*



Note to Figure 8–8:
(1) Simple dual-port RAM supports input and output clock mode in addition to the read and write clock mode shown.

Cyclone II memory blocks support mixed-width configurations, allowing different read and write port widths. Tables 8–5 and 8–6 show the mixed-width configurations.

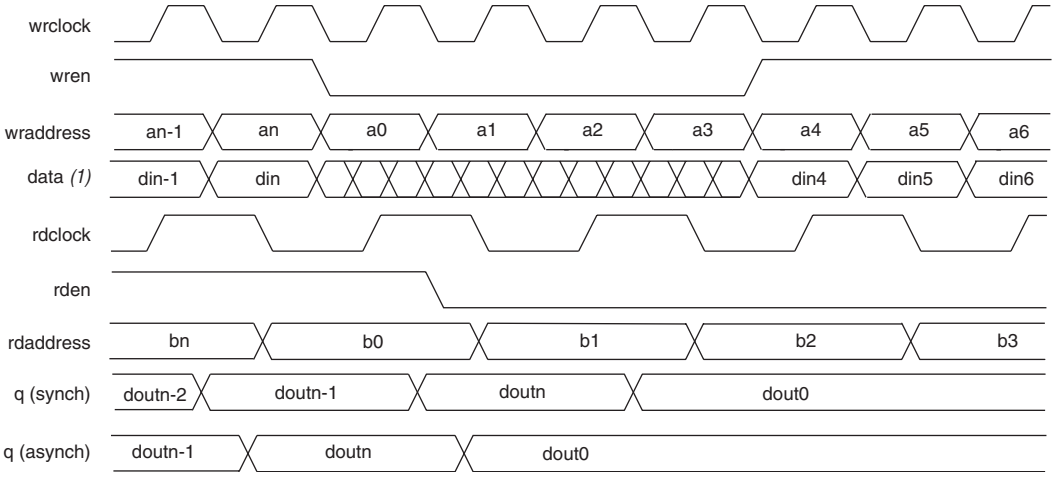
Table 8–5. Cyclone II Memory Block Mixed-Width Configurations (Simple Dual-Port Mode)

Read Port	Write Port								
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
4K × 1	✓	✓	✓	✓	✓	✓			
2K × 2	✓	✓	✓	✓	✓	✓			
1K × 4	✓	✓	✓	✓	✓	✓			
512 × 8	✓	✓	✓	✓	✓	✓			
256 × 16	✓	✓	✓	✓	✓	✓			
128 × 32	✓	✓	✓	✓	✓	✓			
512 × 9							✓	✓	✓
256 × 18							✓	✓	✓
128 × 36							✓	✓	✓

In simple dual-port mode, the memory blocks have one write enable and one read enable signal. They do not support a clear port on the write enable and read enable registers. When the read enable is deactivated, the current data is retained at the output ports. If the read enable is activated during a write operation with the same address location selected, the simple dual-port RAM output is the old data stored at the memory

address. See "Read-During- Write Operation at the Same Address" on page 8–28 for more information. Figure 8–9 shows timing waveforms for read and write operations in simple dual-port mode.

Figure 8–9. Cyclone II Simple Dual-Port Timing Waveforms

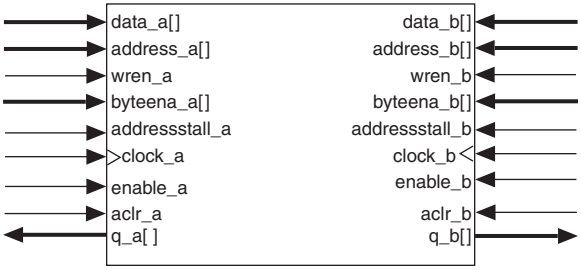


Note to Figure 8–9:
(1) The crosses in the `data` waveform during read mean "don't care."

True Dual-Port Mode

True dual-port mode supports any combination of two-port operations: two reads, two writes, or one read and one write at two different clock frequencies. Figure 8–10 shows Cyclone II true dual-port memory configuration.

Figure 8–10. Cyclone II True Dual-Port Mode *Note (1)*



Note to Figure 8–10:
(1) True dual-port memory supports input and output clock mode in addition to the independent clock mode shown.

The widest bit configuration of the M4K blocks in true dual-port mode is 256 × 16-bit (18-bit with parity).

The 128 × 32-bit (36-bit with parity) configuration of the M4K block is unavailable because the number of output drivers is equivalent to the maximum bit width. The maximum width of the true dual-port RAM equals half of the total number of output drivers because true dual-port RAM has outputs on two ports. Table 8–6 lists the possible M4K block mixed-port width configurations.

Table 8–6. Cyclone II Memory Block Mixed-Port Width Configurations (True Dual-Port)

Read Port	Write Port						
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	512 × 9	256 × 18
4K × 1	✓	✓	✓	✓	✓		
2K × 2	✓	✓	✓	✓	✓		
1K × 4	✓	✓	✓	✓	✓		
512 × 8	✓	✓	✓	✓	✓		
256 × 16	✓	✓	✓	✓	✓		
512 × 9						✓	✓
256 × 18						✓	✓

In true dual-port configuration, the RAM outputs are in read-during-write mode. This means that during a write operation, data being written to the A or B port of the RAM flows through to the A or B

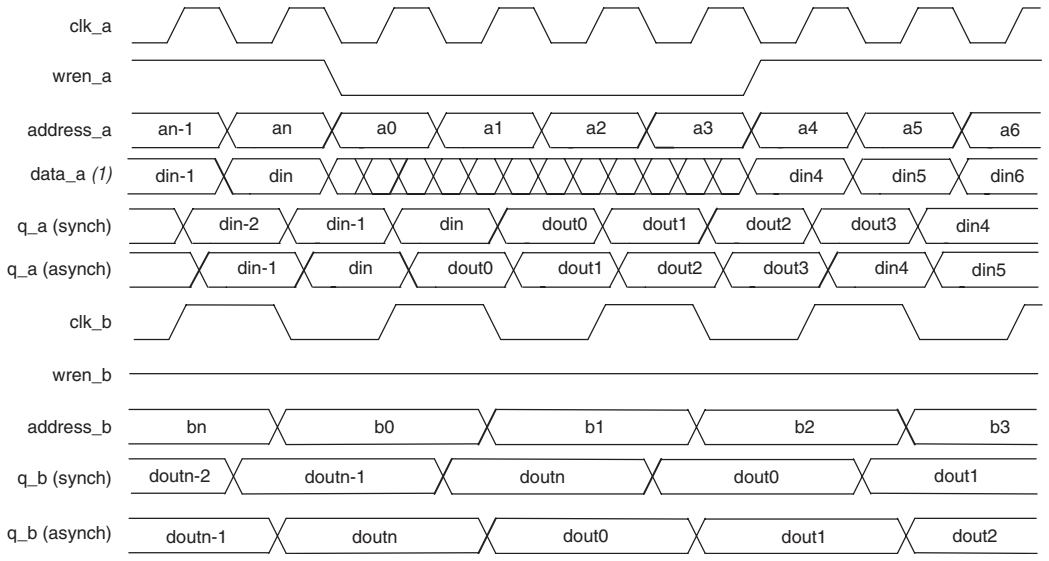
outputs, respectively. When the output registers are bypassed, the new data is available on the rising edge of the same clock cycle on which it was written. See "Read-During- Write Operation at the Same Address" on page 8–28 for waveforms and information on mixed-port read-during-write mode.

Potential write contentions must be resolved external to the RAM because writing to the same address location at both ports results in unknown data storage at that location.

For the maximum synchronous write cycle time, refer to the *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook*.

Figure 8–11 shows true dual-port timing waveforms for the write operation at port A and the read operation at port B.

Figure 8–11. Cyclone II True Dual-Port Timing Waveforms



Note to Figure 8–11:
(1) The crosses in the `data_a` waveform during write indicate "don't care."

Shift Register Mode

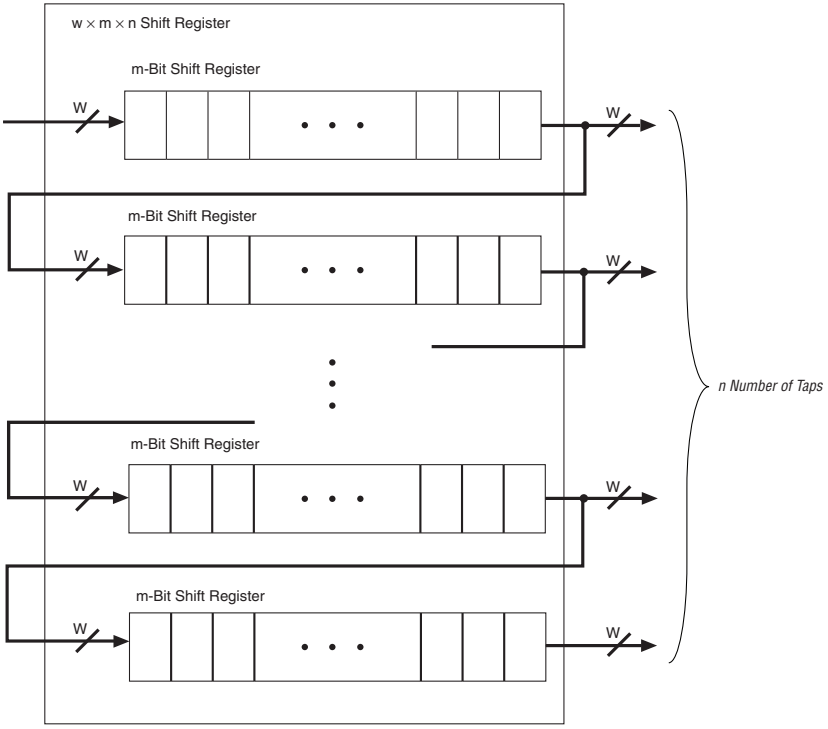
Cyclone II memory blocks can implement shift registers for digital signal processing (DSP) applications, such as finite impulse response (FIR) filters, pseudo-random number generators, multi-channel filtering, and auto-correlation and cross-correlation functions. These and other DSP

applications require local data storage, traditionally implemented with standard flip-flops that quickly exhaust many logic cells for large shift registers. A more efficient alternative is to use embedded memory as a shift register block, which saves logic cell and routing resources.

The size of a ($w \times m \times n$) shift register is determined by the input data width (w), the length of the taps (m), and the number of taps (n), and must be less than or equal to the maximum number of memory bits, which is 4,608 bits. In addition, the size of ($w \times n$) must be less than or equal to the maximum width of the block, which is 36 bits. If a larger shift register is required, the memory blocks can be cascaded.

Data is written into each address location at the falling edge of the clock and read from the address at the rising edge of the clock. The shift register mode logic automatically controls the positive and negative edge clocking to shift the data in one clock cycle. Figure 8–12 shows the Cyclone II memory block in the shift register mode.

Figure 8–12. Cyclone II Shift Register Mode Configuration



ROM Mode

Cyclone II memory blocks support ROM mode. A MIF initializes the ROM contents of these blocks. The address lines of the ROM are registered. The outputs can be registered or unregistered. The ROM read operation is identical to the read operation in the single-port RAM configuration.

FIFO Buffer Mode

A single clock or dual clock FIFO buffer may be implemented in the memory blocks. Dual clock FIFO buffers are useful when transferring data from one clock domain to another clock domain. All FIFO memory configurations have synchronous inputs. However, the FIFO buffer outputs are always combinational (i.e., not registered). Simultaneous read and write from an empty FIFO buffer is not supported.

For more information on FIFO buffers, refer to the *Single- & Dual-Clock FIFO Megafunctions User Guide*.

Clock Modes

Depending on which memory mode is selected, the following clock modes are available:

- Independent
- Input/output
- Read/write
- Single-clock

Table 8–7 shows these clock modes supported by all memory blocks when configured in each respective memory modes.

Table 8–7. Cyclone II Memory Clock Modes

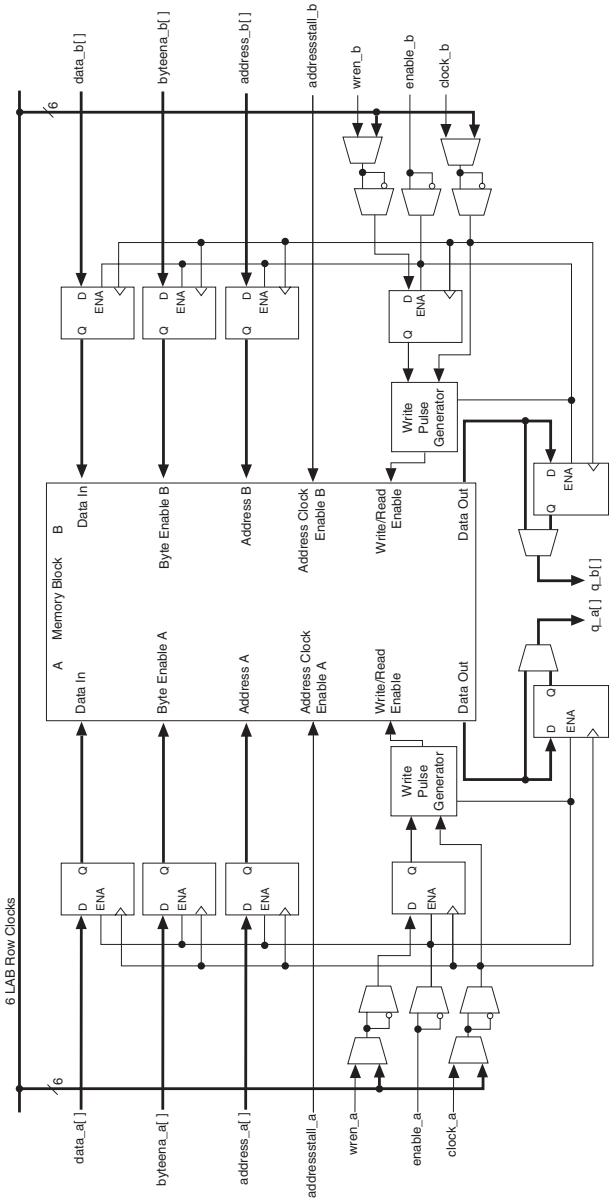
Clocking Modes	True Dual-Port Mode	Simple Dual-Port Mode	Single-Port Mode
Independent	✓		
Input/output	✓	✓	✓
Read/write		✓	
Single clock	✓	✓	✓

Independent Clock Mode

Cyclone II memory blocks can implement independent clock mode for true dual-port memory. In this mode, a separate clock is available for each port (A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side. Each port also supports independent clock enables for port A and B registers. However, ports do not support asynchronous clear signals for the registers.

Figure 8–13 shows a memory block in independent clock mode.

Figure 8–13. Cyclone II Memory Block in Independent Clock Mode *Note (1)*



Note to Figure 8–13:

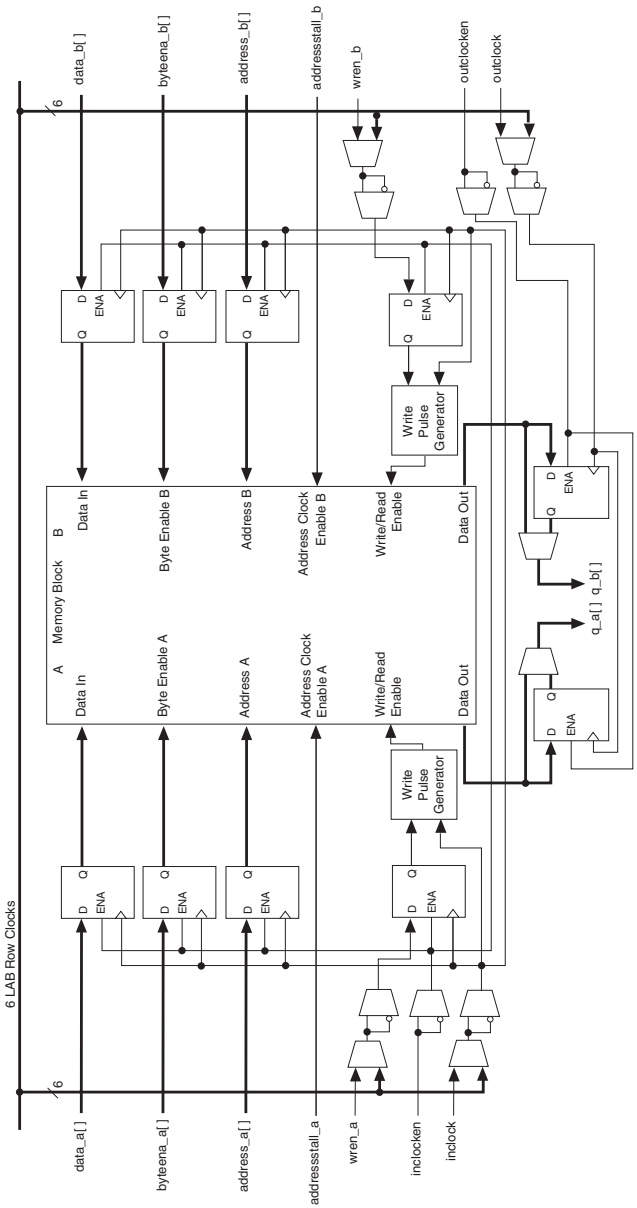
(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

Input/Output Clock Mode

Cyclone II memory blocks can implement the input/output clock mode for true and simple dual-port memory. On each of the two ports, A and B, one clock controls all registers for the data, write enable, and address inputs into the memory block. The other clock controls the blocks' data output registers. Each memory block port also supports independent clock enables for input and output registers. Asynchronous clear signals for the registers are not supported.

Figures 8–14 through 8–16 show the memory block in input/output clock mode for true dual-port, simple dual-port, and single-port modes, respectively.

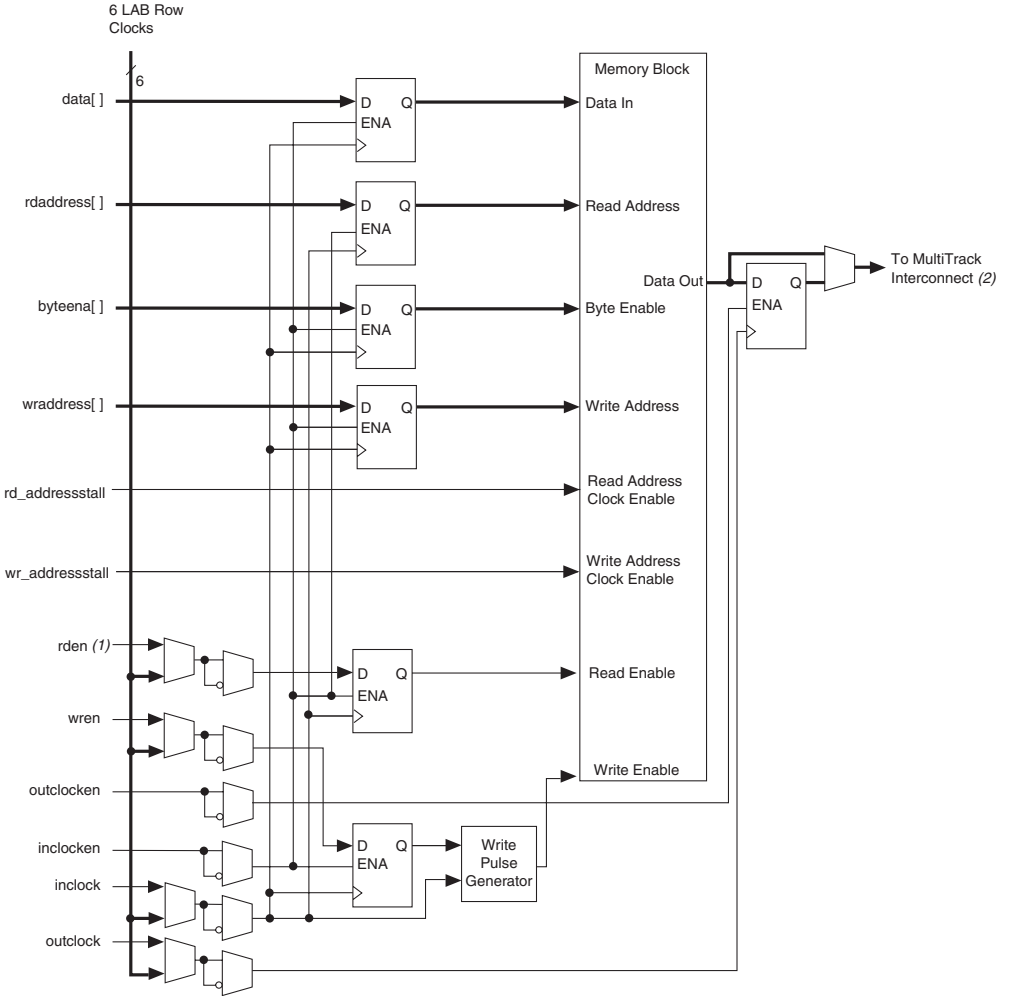
Figure 8–14. Cyclone II Input/Output Clock Mode in True Dual-Port Mode *Note (1)*



Note to Figure 8–14:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

Figure 8–15. Cyclone II Input/Output Clock Mode in Simple Dual-Port Mode *Notes (1), (2)*

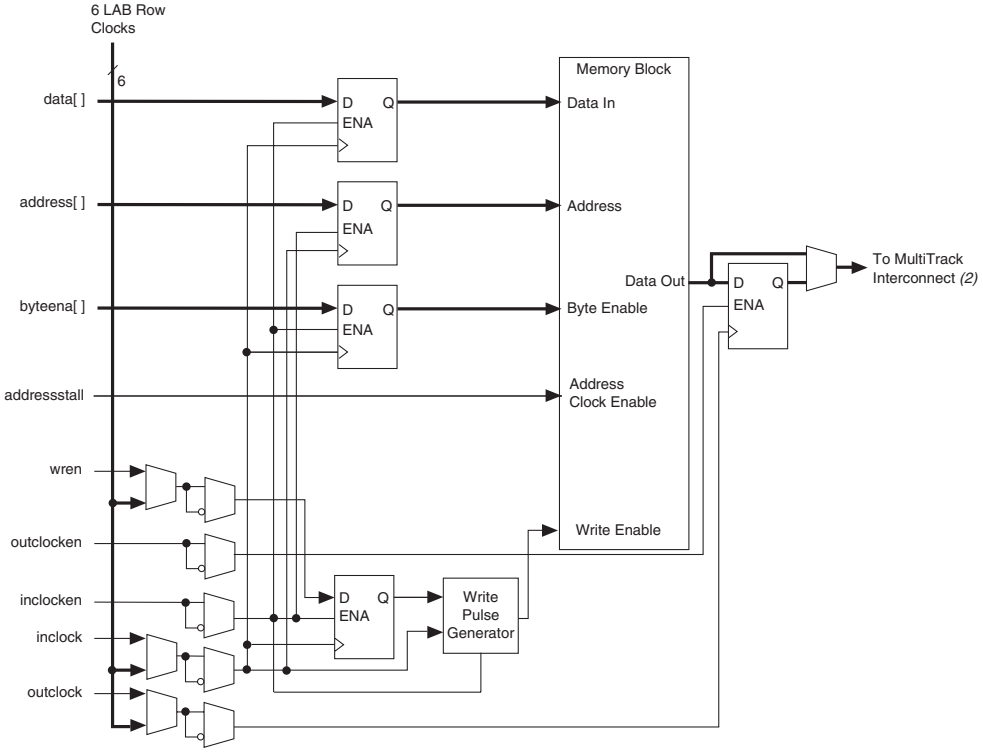


Notes to Figure 8–15:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) See the *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook* for more information on the MultiTrack™ interconnect.

Figure 8–16. Cyclone II Input/Output Clock Mode in Single-Port Mode *Notes (1), (2)*



Notes to Figure 8–16:

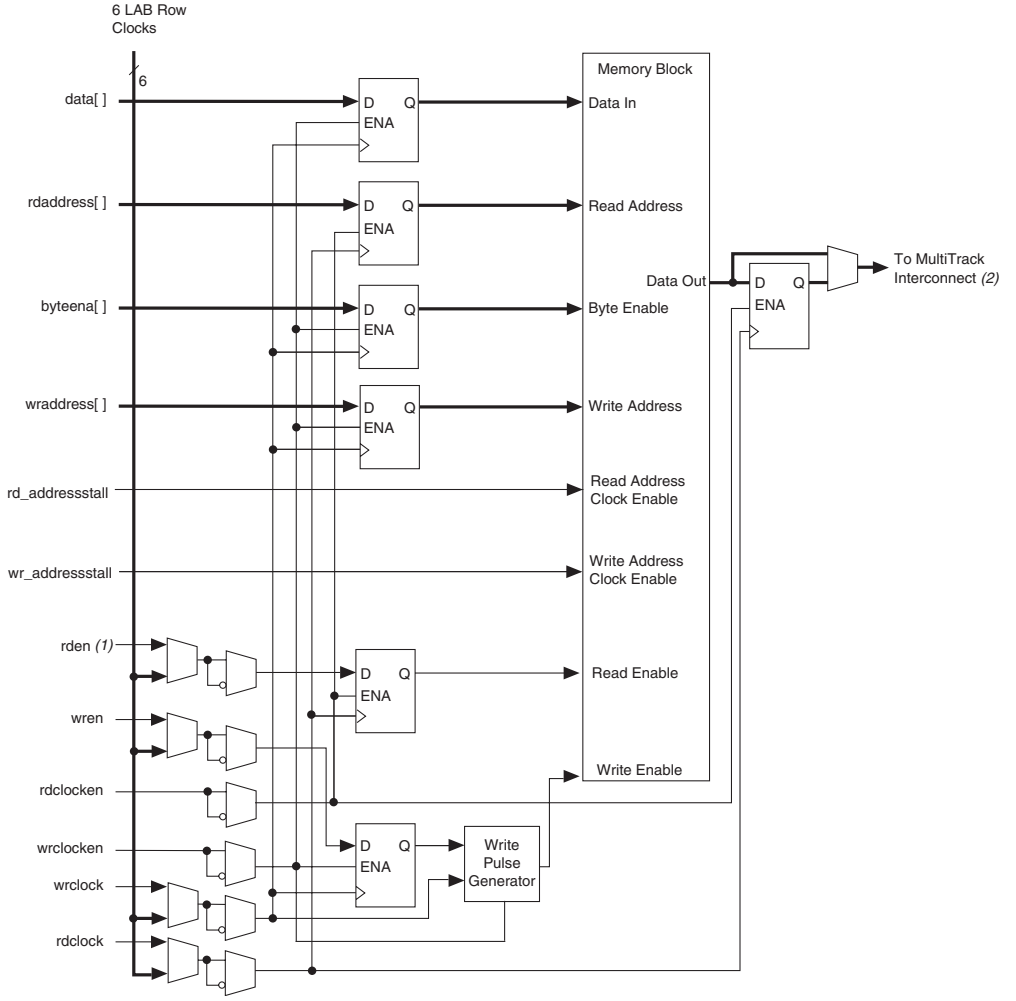
(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) For more information about the MultiTrack interconnect, refer to *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook*.

Read/Write Clock Mode

Cyclone II memory blocks can implement read/write clock mode for simple dual-port memory. The write clock controls the blocks' data inputs, write address, and write enable signals. The read clock controls the data output, read address, and read enable signals. The memory blocks support independent clock enables for each clock for the read- and write-side registers. This mode does not support asynchronous clear signals for the registers. Figure 8–17 shows a memory block in read/write clock mode.

Figure 8–17. Cyclone II Read/Write Clock Mode *Notes (1), (2)*



Notes to Figure 8–17:

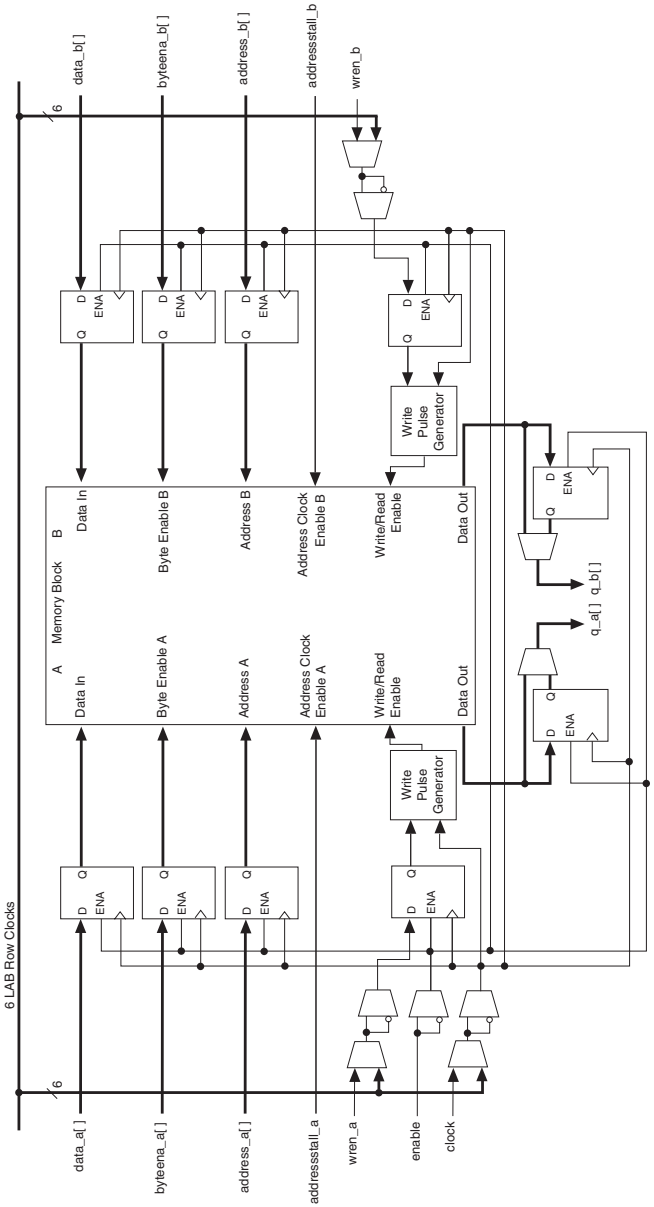
(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) For more information about the MultiTract interconnect, refer to *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook*.

Single-Clock Mode

Cyclone II memory blocks support single-clock mode for true dual-port, simple dual-port, and single-port memory. In this mode, a single clock, together with a clock enable, controls all registers of the memory block. This mode does not support asynchronous clear signals for the registers. Figures 8–18 through 8–20 show the memory block in single-clock mode for true dual-port, simple dual-port, and single-port modes, respectively.

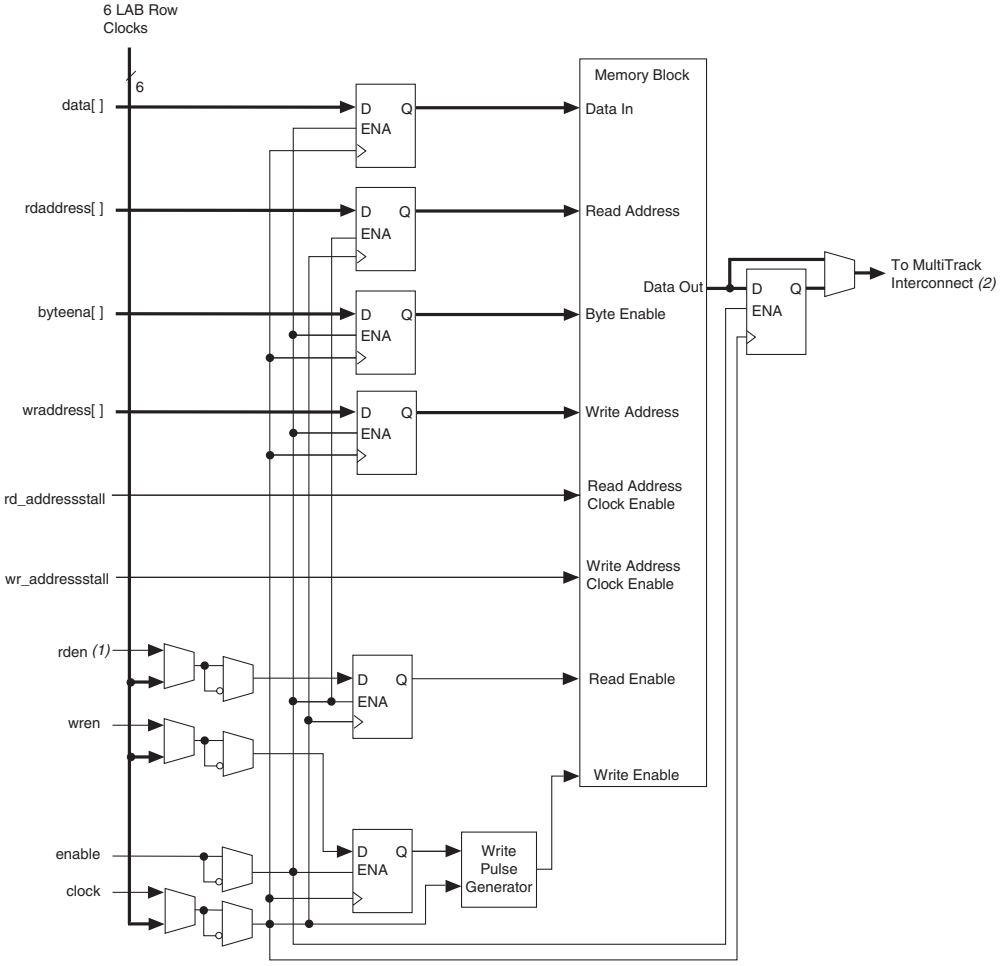
Figure 8–18. Cyclone II Single-Clock Mode in True Dual-Port Mode *Note (1)*



Note to Figure 8–18:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

Figure 8–19. Cyclone II Single-Clock Mode in Simple Dual-Port Mode *Notes (1), (2)*

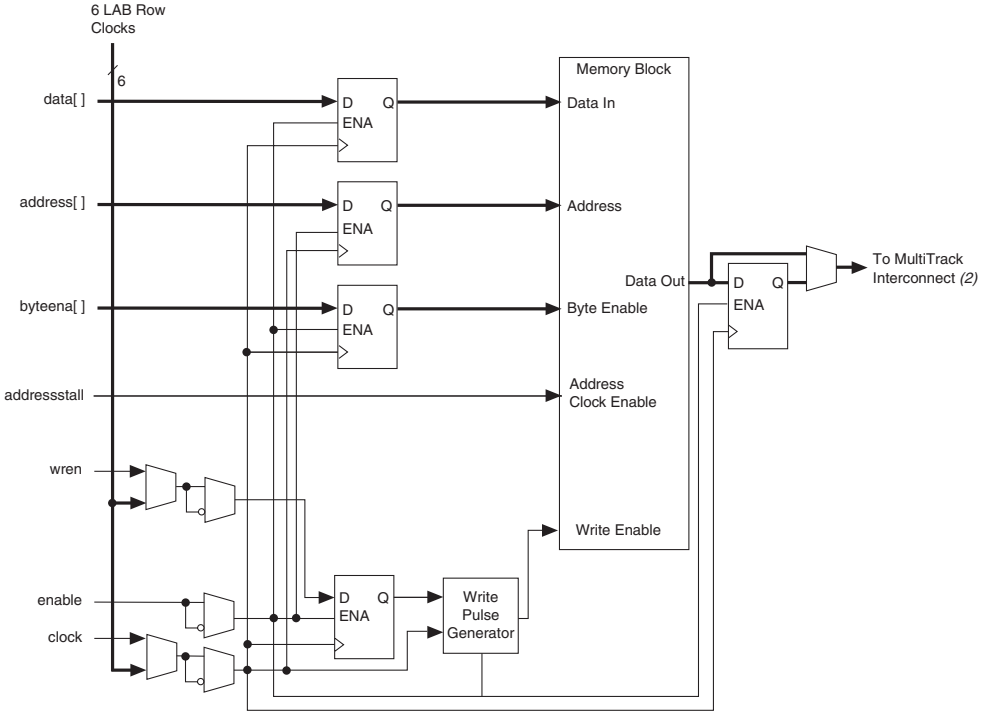


Notes to Figure 8–19:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) See the *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook* for more information on the MultiTrack interconnect.

Figure 8–20. Cyclone II Single-Clock Mode in Single-Port Mode *Notes (1), (2)*



Notes to Figure 8–20:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) See the *Cyclone II Device Family Data Sheet* in Volume 1 of the *Cyclone II Device Handbook* for more information on the MultiTrack interconnect.

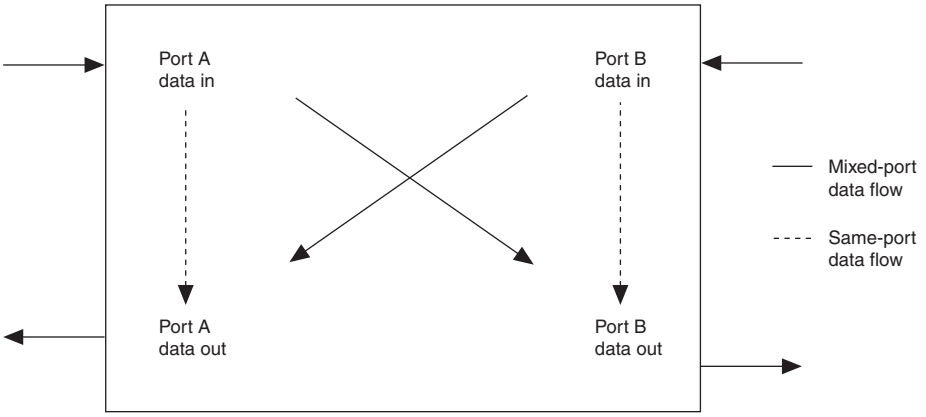
Power-Up Conditions & Memory Initialization

The Cyclone II memory block outputs always power-up to zero, regardless of whether the output registers are used or bypassed. Even if an MIF pre-loads the contents of the memory block, the outputs still power up cleared. For example, if address 0 is pre-initialized to `FF`, M4K blocks power up with the output at `00`. A subsequent read after power up from address 0 outputs the pre-initialized value of `FF`.

Read-During-Write Operation at the Same Address

The "Same-Port Read-During-Write Mode" and "Mixed-Port Read-During-Write Mode" sections describe the functionality of the various RAM configurations when reading from an address during a write operation at that same address. There are two read-during-write data flows: same-port and mixed-port. Figure 8–21 shows the difference between these flows.

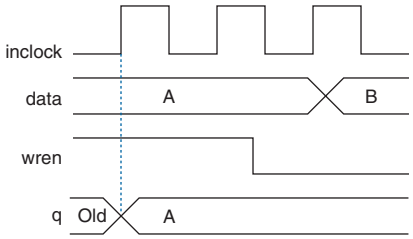
Figure 8–21. Cyclone II Read-During-Write Data Flow



Same-Port Read-During-Write Mode

For read-during-write operation of a single-port RAM or the same port of a true dual-port RAM, the new data is available on the rising edge of the same clock cycle on which it was written. Figure 8–22 shows a sample functional waveform. When using byte enables in true dual-port RAM mode, the outputs for the masked bytes on the same port are unknown (see Figure 8–2 on page 8–6). The non-masked bytes are read out as shown in Figure 8–22.

Figure 8–22. Cyclone II Same-Port Read-During-Write Functionality *Note (1)*



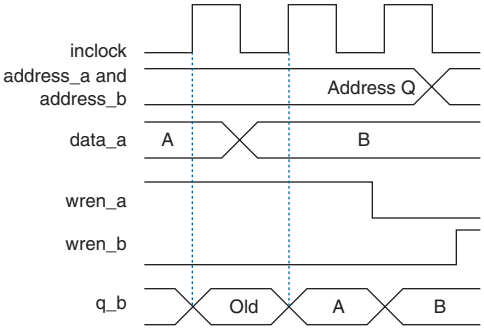
Note to Figure 8–22:
(1) Outputs are not registered.

Mixed-Port Read-During-Write Mode

This mode applies to a RAM in simple or true dual-port mode, which has one port reading and the other port writing to the same address location with the same clock.

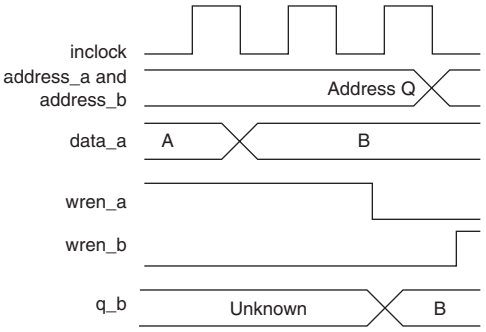
In this mode, you also have two output choices: old data or don't care. In Old Data Mode, a read-during-write operation to different ports causes the RAM outputs to reflect the old data at that address location. In Don't Care Mode, the same operation results in a "don't care" or unknown value on the RAM outputs.

Figure 8–23. Cyclone II Mixed-Port Read-During-Write: Old Data Mode *Note (1)*



Note to Figure 8–23:
(1) Outputs are not registered.

Figure 8–24. Cyclone II Mixed-Port Read-During-Write: Don't Care Mode *Note (1)*



Note to Figure 8–24:
(1) Outputs are not registered.

Mixed-port read-during-write is not supported when two different clocks are used in a dual-port RAM. The output value is unknown during a mixed-port read-during-write operation.

Conclusion

The M4K memory structure of Cyclone II devices provides a flexible memory architecture with high memory bandwidth. It addresses the needs of different memory applications in FPGA designs with features such as different memory modes, byte enables, parity bit storage, address clock enables, mixed clock mode, shift register mode, mixed-port width support, and true dual-port mode.

Referenced Documents

This chapter references the following documents:

- *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook*
- *Single- and Dual-Clock FIFO Megafunction User Guide*
- *Using Parity to Detect Errors White Paper*

Document Revision History

Table 8–8 shows the revision history for this document.

Table 8–8. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2008 v2.4	Corrected Figure 8–12.	—
February 2007 v2.3	• Added document revision history. • Updated "Packed Mode Support" section. • Updated "Mixed-Port Read-During-Write Mode" section and added new Figure 8–24.	• In packed mode support, the maximum data width for each of the two memory block is 18 bits wide. • Added don't care mode information to mixed-port read-during-write mode section.
November 2005 v2.1	Updated Figures 8–13 through 8–20.	—
July 2005 v2.0	Added Clear Signals section.	—
February 2005 v1.1	Added a note to Figures 8-13 through 8-20 regarding violating the setup and hold time on address registers.	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—